UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

TRENCHANT BLADE TECHNOLOGIES LLC, Plaintiff, v. INTEL CORPORATION, Defendant.	§ § § § § § § § § § §	Case No. **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Trenchant Blade Technologies LLC ("Trenchant"), by and through its attorneys, for its Complaint against Defendant Intel Corporation ("Intel"), and demanding trial by jury, hereby alleges, on information and belief with regard to the actions of Intel and on knowledge with regard to its own actions, as follows:

I. NATURE OF THE ACTION

1. This is an action for patent infringement arising under the patent laws of the United States, 35 U.S.C. §§ 271, *et seq*., to enjoin and obtain damages resulting from Defendant's unauthorized use, sale, and offer to sell in the United States, of products, methods, processes, services and/or systems that infringe Plaintiff's United States patents, as described herein.

2. Defendant manufactures, provides, uses, sells, offers for sale, imports, and/or distributes infringing products and services, and encourages others to use its products and services in an infringing manner, as set forth herein.

3. Plaintiff seeks, among other relief, past and future damages and prejudgment and post-judgment interest for Defendant's infringement of the Asserted Patents, as defined below.

II. PARTIES

4. Plaintiff Trenchant Blade Technologies LLC is a limited liability company organized and existing under the laws of the State of Texas, with its principal place of business located at 5204 Bluewater Drive, Frisco, Texas 75034.

5. Trenchant is the owner of the entire right, title, and interest of the Asserted Patents, as defined below, including the right to sue for and collect past, present, and future damages and to seek and obtain injunctive or any other relief for infringement.

6. Defendant Intel Corporation is a Delaware corporation with its principal place of business at 2200 Mission College Boulevard, Santa Clara, California 95054.

7. On information and belief, Intel is registered to do business in the State of Texas and has been since at least April 1989. Defendant may be served by serving its registered agent, C T Corporation System, 1999 Bryan St., Ste. 900, Dallas, TX 75201-3136.

8. On information and belief, Intel has places of business at 9442 N. Capital of Texas Hwy., Bldg. 2, Suite 600, Austin, Texas 78759; and 1300 S. Mopac Expressway, Austin, Texas 78746 (collectively, "Intel Austin Offices").

III. JURISDICTION AND VENUE

9. This is an action for patent infringement which arises under the patent laws of the United States, in particular, 35 U.S.C. §§ 271, 281, 283, 284, and 285.

10. This Court has exclusive jurisdiction over the subject matter of this action under 28 U.S.C. §§ 1331, 1332, and 1338(a).

11. This Court has personal jurisdiction over Defendant in this action pursuant to due process and/or the Texas Long Arm Statute, by virtue of at least the substantial business Defendant conducts in this forum, directly and/or through intermediaries, including but not limited to: (1) having committed acts within the Western District of Texas giving rise to this action and having established minimum contacts with this forum such that the exercise of jurisdiction over Defendant would not offend traditional notions of fair play and substantial justice; (2) having directed its activities to customers in the State of Texas and this District, solicited business in the State of Texas and this District, transacted business within the State of Texas and this District and attempted to derive financial benefit from residents of the State of Texas and this District, including benefits directly related to the instant patent infringement causes of action set forth herein; (3) having placed its products and services into the stream of commerce throughout the United States and having been actively engaged in transacting business in Texas and in this District; and (4) either individually, as members of a common business enterprise, and/or in conjunction with third parties, having committed acts of infringement within Texas and in this District.

12. Defendant has committed and continues to commit acts of infringement in this District directly and through third parties by, among other things, making, selling, advertising (including through websites), offering to sell, distributing, and/or importing products and/or services that infringe the Asserted Patents as defined below.

13. Defendant has, directly or through its distribution network, purposefully and voluntarily placed infringing products in the stream of commerce knowing and expecting them to be purchased and used by consumers in Texas.

14. Defendant has committed direct infringement in Texas.

15. Defendant has committed indirect infringement based on acts of direct infringement in Texas.

16. Defendant has transacted, and as of the time of filing of the Complaint, continues to transact business within this District.

17. Defendant derives substantial revenues from its infringing acts in this District, including from its manufacture and sale of infringing products in the United States.

18. In sum, this Court has specific and general personal jurisdiction over Defendant because, *inter alia*, Defendant, on information and belief: (1) has substantial, continuous, and systematic contacts with this State and this judicial district; (2) owns, manages, and operates facilities in this State and this judicial district; (3) enjoys substantial income from sales in this State and this judicial

district; (4) employs Texas residents in this State and this judicial district, and (5) markets products in this State and judicial district.

19. On information and belief, Defendant has at least two regular and established places of business in this District, including at the Intel Austin Offices. On information and belief, Intel has developed products, including memory and other integrated circuits, at its Austin Design Center in Austin, Texas for many years.

20. Venue is proper against Defendant in this District pursuant to 28 U.S.C. § 1400(b) because it has committed acts of infringement in this District and maintains a regular and established place of business in this District, at least at Intel's Austin Offices.

IV. COUNTS OF PATENT INFRINGEMENT

21. Plaintiff alleges that Defendant has infringed and continues to infringe the following United States patents (collectively, the "Asserted Patents"):

United States Patent No. 6,720,619 (the "'619 Patent") (Exhibit A)
United States Patent No. 7,056,821 (the "'821 Patent") (Exhibit B)
United States Patent No. 7,498,642 (the "'642 Patent") (Exhibit C)
United States Patent No. 7,511,332 (the "'332 Patent") (Exhibit D)

COUNT ONE
INFRINGEMENT OF U.S. PATENT 6,720,619

22. Plaintiff incorporates by reference the allegations in all preceding paragraphs as if fully set forth herein.

23. The '619 Patent, entitled "SEMICONDUCTOR-ON-INSULATOR CHIP INCORPORATING PARTIALLY-DEPLETED, FULLY-DEPLETED, AND

MULTIPLE-GATE DEVICES," was filed on December 13, 2002 and duly and legally issued by the United States Patent and Trademark Office on April 13, 2004.

24. The '619 Patent claims patent-eligible subject matter and is valid and enforceable.

Technical Description and Background

25. The '619 Patent is directed to field effect transistors. Transistors are semiconductor devices that are formed on wafers, which are made by foundries. Wafers contain multiple, identical chips which are designed by chip designers. Individual chips are cut from wafers and packaged. Those chips go into a variety of consumer products, such as smartphones, tablets, personal computers, and automobile parts and components.

26. Specifically, the '619 Patent claims an improved multiple-gate device structure. The patent explains improvements in the context of partially depleted semiconductor-on-insulator (PD-SOI) chips, for example. The '619 Patent notes that, while progress had been made in PD-SOI technology, significant design burden was faced by its users because of "floating body effects. In PD-SOI devices, charge carriers generated by impact ionization near the drain/source region accumulate near the source/drain region of the transistor. When sufficient carriers accumulate in the floating body, which is formed right below the channel region, the body potential is effectively altered. Floating body effects occur in PD-SOI devices because of charge build-up in the floating body region. This results in kinks in the device current-voltage (I-V) curves, thereby degrading the electrical performance of the circuit. In

general, the body potential of a PD-SOI device may vary during static, dynamic, or transient device operation, and is a function of many factors like temperature, voltage, circuit topology, and switching history. Therefore, circuit design using PD-SOI devices is not straightforward, and there is a significant barrier for the adoption of PD-SOI technology or the migration from bulk-Si design to PD-SOI design." '619 Patent, 1:40-60. The '619 Patents notes several "traditional" ways exist to suppress floating body effects but faults multiple shortcomings that exist with these methods. '619 Patent, 1:61-2:32.

27. The '619 patent improves upon the prior art by disclosing a new technology useful for suppressing floating body effects "not by reducing the silicon body thickness, but by rearranging the planar transistor geometry, channel length, or channel width." '619 Patent, 3:46-56.

Direct Infringement

28. Defendant without authorization or license from Plaintiff, has been and is directly infringing the '619 Patent, either literally or equivalently, as infringement is defined by 35 U.S.C. § 271, including through making, using (including for testing purposes), designing, manufacturing, importing, distributing, selling, and offering for sale chips, processors, and other electronic devices and products that infringe one or more claims of the '619 Patent. Defendant is thus liable for direct infringement pursuant to 35 U.S.C. § 271.

29. Exemplary infringing products include Intel processors and chips, including but not limited to the Intel's integrated circuit devices made using the Intel

10 nm and 14 nm advanced node FinFET transistors process as shown, for example, in Intel i3-812U Cannon using Intel's 10 nm node FinFET high-k metal gate (HKMG) CMOS process and Intel Broadwell SR217 Core M-5Y10 Microprocessor using 14 nm node FinFET transistor manufacturing process, and similar products, hereinafter "'619 Accused Products."

30. Plaintiff names these exemplary infringing instrumentalities to serve as notice of Defendant's infringing acts, but Plaintiff reserves the right to name additional infringing products, known to or learned by Plaintiff or revealed during discovery, and include them in the definition of '619 Accused Products.

31. As a specific, nonlimiting example, Defendant is liable for direct infringement pursuant to 35 U.S.C. § 271 for the manufacture, sale, offer for sale, importation, or distribution of the Intel Kaby Lake Core i5 7200U Microprocessor Intel 14 nm+ Tri-Gate HKMG CMOS Process, hereinafter "'619 Exemplary Accused Product." The '619 Exemplary Accused Product meets all limitations of, for example, claim 1 of the '619 Patent, either literally or under the doctrine of equivalents.

32. The '619 Exemplary Accused Product is a multiple-gate device structure comprising a substrate and a semiconductor depletion material with a first predetermined height and width overlying a predetermined portion of the substrate to form an active region:

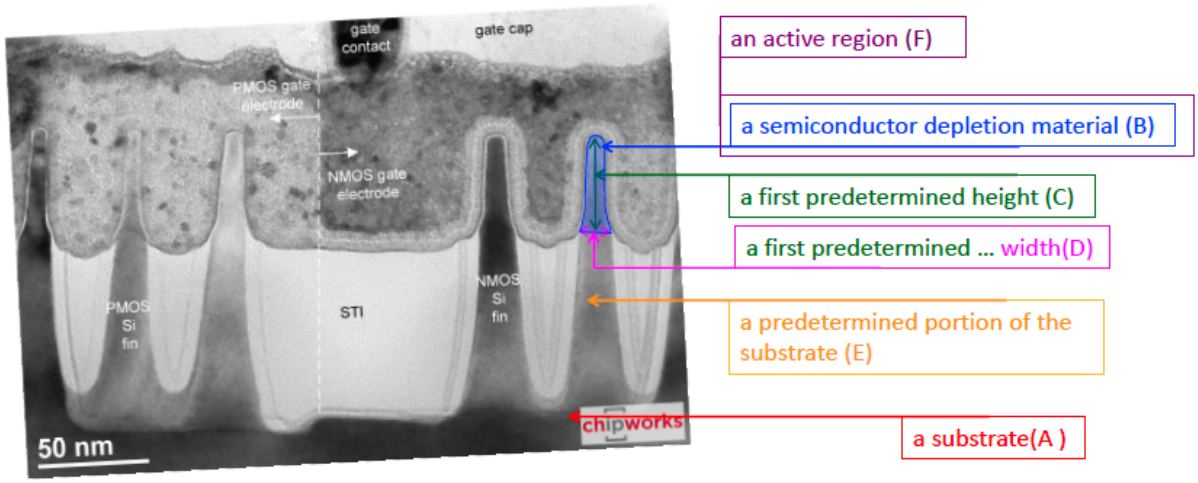

Figure 1: Cross-Sectional TEM Image of the Intel 14 nm FinFET Transistors (Parallel to Gate Electrode)

33. The '619 Exemplary Accused Product further comprises an isolation material formed on top of the substrate surrounding the active region so as to bury a bottom portion of the active region therein, thereby exposing a top portion of the active region:

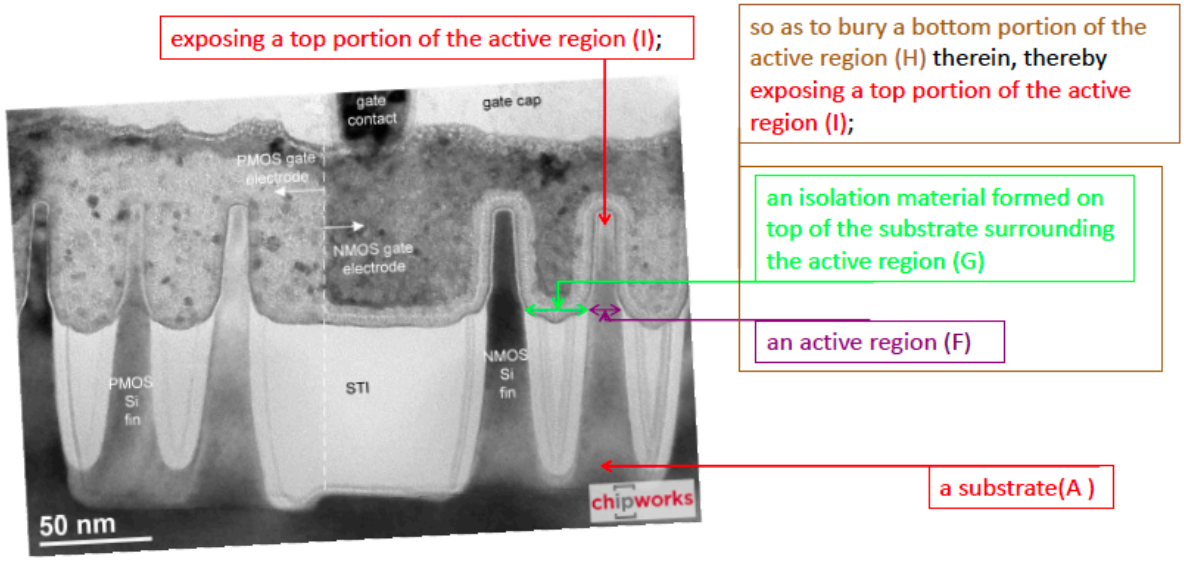

Figure 2: Cross-Sectional TEM Image of the Intel 14 nm FinFET Transistors (Parallel to Gate Electrode)

34. The ’619 Exemplary Accused Product further comprises a gate dielectric layer covering the exposed portion of the top and two sidewalls of the top portion of the active region, and at least one gate electrode formed on top of the gate dielectric layer and extending through two sidewalls thereof to reach the isolation material:

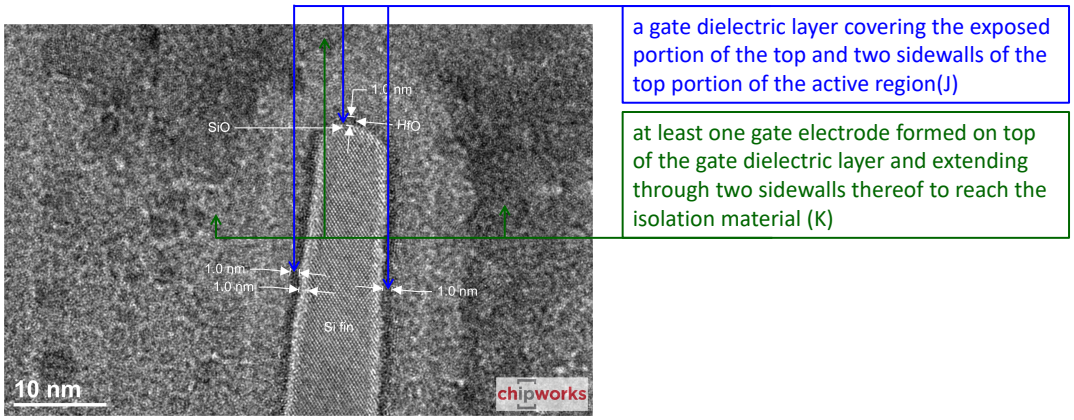

Figure 3: Cross-Sectional TEM Image of the Intel 14 nm FinFET NMOS Transistors (Parallel to Gate Electrode)

35. The source and drain regions of the ’619 Exemplary Accused Product are separated by the gate electrode:

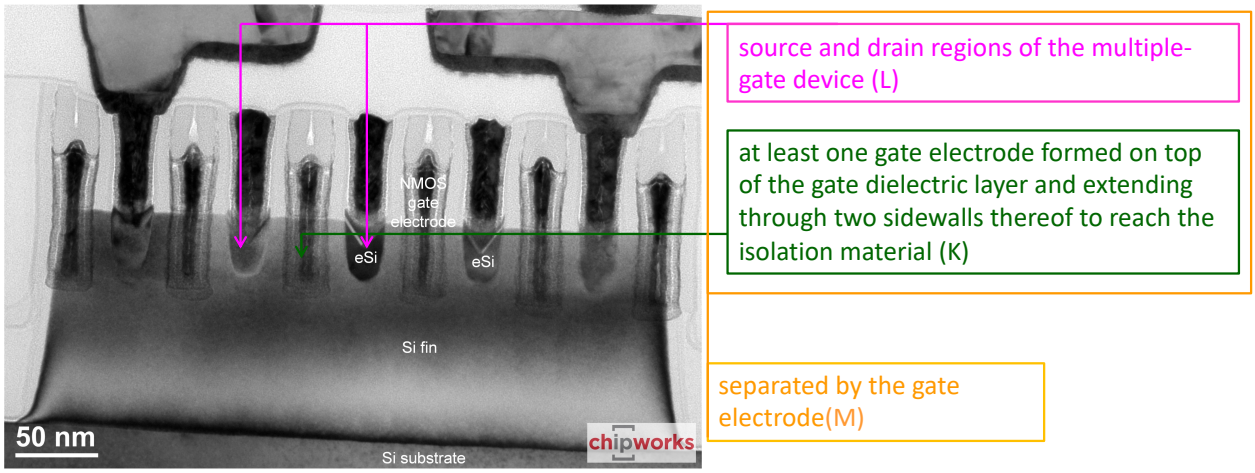

Figure 4: Cross-Sectional TEM Image of the Intel 14 nm FinFET NMOS Transistors (Perpendicular to Gate Electrode)

36. The exposed top region of the active region has its top corners rounded:

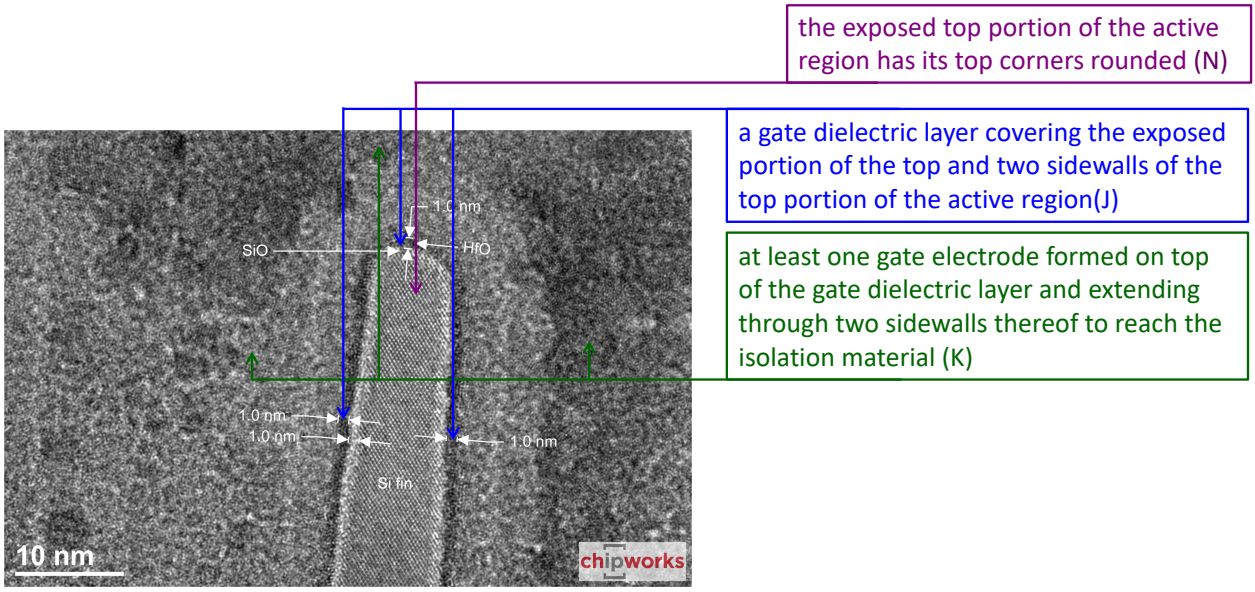

Figure 5: Cross-Sectional TEM Image of the Intel 14 nm FinFET NMOS Transistors (Parallel to Gate Electrode)

Willful Infringement

37. Defendant had actual knowledge of the '619 Patent and its infringement thereof at least as of receipt of Plaintiff's notice letters dated April 19, 2020 and/or March 26, 2021.

38. Defendant has numerous lawyers and other active agents of Defendant who regularly review patents and published patent applications relevant to technology in the fields of the Asserted Patent.

39. Defendant has been issued many thousands of patents held in the name of the Defendant or a related entity, many of which are patents prosecuted in the USPTO in the same technology area as the '619 Patent, giving Defendant intimate knowledge of the art in fields relevant to this civil action. The timing, circumstances and extent of Defendant obtaining actual knowledge of the '619 Patent prior to the commencement of this lawsuit will be confirmed during discovery.

40. Defendant's infringement of the Asserted Patents was either known or was so obvious that it should have been known to Defendant.

41. Notwithstanding this knowledge, Defendant has knowingly or with reckless disregard infringed the '619 Patent. Defendant continued to commit acts of infringement despite being on notice of infringement and aware of an objectively high likelihood that its actions constitute infringement of Plaintiff's valid patent rights, either literally or equivalently.

42. Defendant is therefore liable for willful infringement and Plaintiff accordingly seeks enhanced damages pursuant to 35 U.S.C. §§ 284 and 285.

Indirect, Induced, and Contributory Infringement

43. Defendant, directly and/or through its subsidiaries, affiliates, agents, and/or business partners, has committed and continue to commit acts of indirect infringement of at least one claim of the '619 Patent, pursuant to 35 U.S.C. §§ 271(b) and (c) by actively inducing or contributing to the acts of direct infringement performed by others in the United States, the State of Texas, and the Western District of Texas.

44. Defendant has induced and continues to induce through affirmative acts its distributors, manufacturers, testers, customers, and/or end users, such as designers of Defendant's chips and end users of Defendant's chips to directly infringe the '619 Patent by making, using, selling, and/or importing the '619 Accused Products, with the specific intent to induce acts constituting infringement, and

knowing that the induced acts constitute patent infringement, either literally or equivalently.

45. Defendant has knowingly contributed to direct infringement by its customers through affirmative acts and by having imported, sold, and/or offered for sale, and knowingly importing, selling, and/or offering to sell within the United States the '619 Accused Products which are not suitable for substantial non-infringing use and which are especially made or especially adapted for use by its customers in an infringement of the asserted patent.

46. The affirmative acts of inducement by Defendant include, but are not limited to, any one or a combination of: (i) designing infringing chips for manufacture according to specification; (ii) collaborating on and/or funding the development of the infringing chips and/or technology; (iii) soliciting and sourcing the manufacture of infringing chips; licensing and transferring technology and know-how to enable the manufacture of infringing chips; (v) enabling and encouraging the use, sale, or importation of infringing chips by its customers; (vi) advertising the infringing chips and/or technology; and (vii) providing data sheets, technical guides, demonstrations, software and hardware specifications, installation guides, product specifications, user manuals, marketing materials, and instructions, including on Defendant's website, https://www.intel.com.

47. Defendant has contributed and continues to contribute to the direct infringement of the '619 Patent its customers, and other third parties; and Defendant, its customers, and other third parties do directly infringe.

48. Defendant imports, exports, makes or sells parts, components, or intermediate products to customers and third parties that, once assembled, infringe the '619 Patent by the sale and/or use of the assembled processors and/or devices.

49. Defendant makes, uses, sells, and/or offers to sell infringing semiconductor devices and/or processor chips, which are especially made to design and specification, and are not staple products or commodities with substantial non-infringing use.

50. Defendant knew that the induced conduct would constitute infringement and intended that infringement at the time of committing the aforementioned acts, such that the acts and conduct have been and continue to be committed with the specific intent to induce infringement, or deliberately avoiding learning of the infringing circumstances at the time of committing these acts so as to be willfully blind to the infringement that was induced.

51. As a result of Defendant's infringement, Plaintiff has suffered monetary damages, and is entitled to an award of damages adequate to compensate it for such infringement which, by law, can be no less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

52. Plaintiff has incurred and will continue to incur substantial damages, including monetary damages.

COUNT TWO
INFRINGEMENT OF U.S. PATENT 7,056,821

53. Plaintiff incorporates by reference the allegations in all preceding paragraphs as if fully set forth herein.

54. The ’821 Patent, entitled “METHOD FOR MANUFACTURING DUAL DAMASCENE STRUCTURE WITH A TRENCH FORMED FIRST,” was filed on August 17, 2004 and duly and legally issued by the United States Patent and Trademark Office on June 6, 2006.

55. The ’821 Patent claims patent-eligible subject matter and is valid and enforceable.

Technical Description and Background

56. The ’821 Patent is directed to an integrated circuit having a dual damascene structure. At the time of invention, the “dual damascene process [had been] developed for forming via plugs and metal interconnects at the same time.” ’821 Patent, 1:14-26. Conventional methods were “to form a trench following a via. This method, however, conceals some problems… the metal layer [is] exposed to air before the sacrificial layer is filled. Using copper as the metal layer dramatically affects the quality of the devices, since copper is inclined to oxidize… Moreover, micro trenches and fences issues commonly occur in the conventional process…that affect the subsequent processes. For example, fences cause poor coverage capability of barrier layers and electrochemical plating (ECP) deposition. Fences, for instance, further result in unsteady electrical properties, as well as poor reliability of devices. In addition, the dielectric layer is generally constituted by porous low-k materials, through which residual NH-group components in the substrate readily pass to neutralize with the photoresist layer, and consequently react to be photoresist scum.

Therefore, the photoresist is not developed and patterned well, which also leads to a decrease in the production yield." '821 Patent, 1:59-2:14.

57. The '821 Patent "provide[s] a method for manufacturing a dual damascene structure with a trench formed first, in order to reduce Q-time when copper is exposed to the air and also to simplify the process by omitting a post-baking step following etching a via. [The] invention improve[s] the surface quality of the photoresist layer for etching a via by planarizing the sacrificial layer. The photolithography process thus has a wider control window. No photoresist scum issue is caused by neutralization of the photoresist with NH— group components due to the greater open area of the trench. The photoresist is therefore patterned and transferred more clearly and more precisely." The patent also provides a method for "reducing micro trenches and fences by means of a sacrificial layer with substantially the same etching rate selectivity as an inter-metal dielectric layer; both of which and the photoresist are consequently easily stripped by a wet or dry cleaning process or by a wet or dry etching process." '821 Patent, 2:18-40.

Direct Infringement

58. Defendant without authorization or license from Plaintiff, has been and is directly infringing the '821 Patent, either literally or equivalently, as infringement is defined by 35 U.S.C. § 271, including through making, using (including for testing purposes), designing, manufacturing, importing, distributing, selling, and offering for sale chips, processors, and other electronic devices and products that are made by a method that infringe one or more claims of the '821 Patent. Defendant further

provides services that practice methods that infringe one or more claims of the '821 Patent. Defendant is thus liable for direct infringement pursuant to 35 U.S.C. § 271.

59. Exemplary infringing products include Intel processors and chips, including but not limited to the Intel's integrated circuit devices made using the Intel 10 nm, 14 nm and 20 nm advanced process nodes as shown, for example, in Intel i3-812U Cannon Lake using Intel's 10 nm node FinFET high-k metal gate (HKMG) CMOS process and Intel Broadwell SR217 Core M-5Y10 Microprocessor using 14 nm node FinFET transistor manufacturing process, and similar products, hereinafter "'821 Accused Products."

60. Plaintiff names these exemplary infringing instrumentalities to serve as notice of Defendant's infringing acts, but Plaintiff reserves the right to name additional infringing products, known to or learned by Plaintiff or revealed during discovery, and include them in the definition of '821 Accused Products.

61. As a specific, nonlimiting example, Defendant is liable for direct infringement pursuant to 35 U.S.C. § 271 for the manufacture, sale, offer for sale, importation, or distribution of the Intel Kaby Lake Core i5 7200U Microprocessor Intel 14 nm+ Tri-Gate HKMG CMOS Process, hereinafter "'821 Exemplary Accused Product." The '821 Exemplary Accused Product is made by a method that meets all limitations of, for example, claim 1 of the '821 Patent, either literally or under the doctrine of equivalents.

62. The '821 Exemplary Accused Product is a manufactured dual damascene structure with a trench formed first, made by providing a substrate having a plurality of semiconductor devices and forming a first metal layer on the substrate:

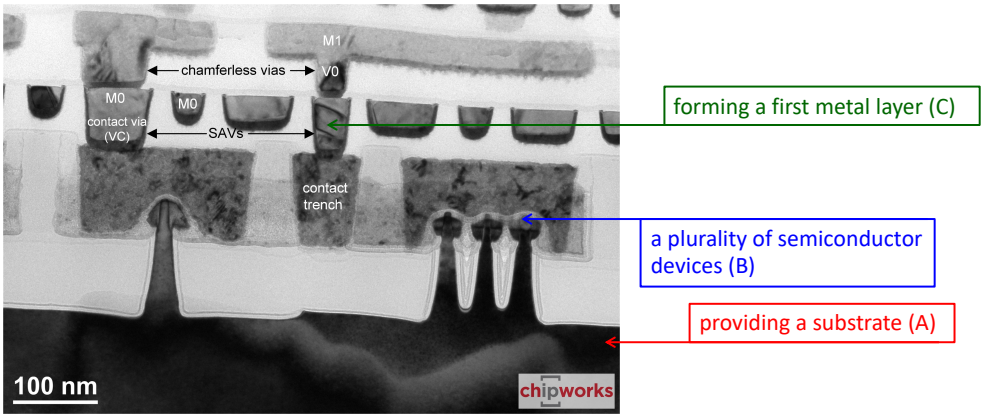

Figure 6: Cross-Sectional TEM Image of the Intel 14 nm FinFET Kaby Lake Die

63. The '821 Exemplary Accused Product is made by forming a first etching stop layer on the first metal layer and forming a dielectric layer on the first etching stop layer:

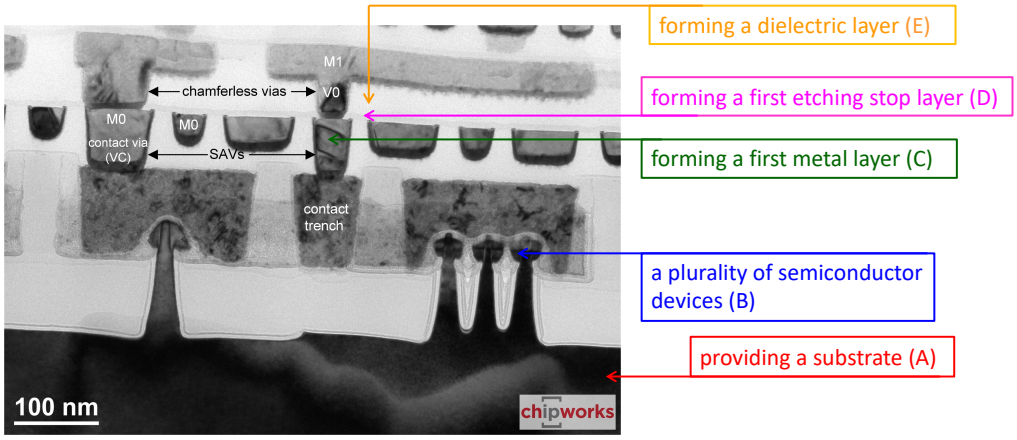

Figure 7: Cross-Sectional TEM Image of the Intel 14 nm FinFET Kaby Lake Die

64. The ’821 Exemplary Accused Product is made by forming a second etching stop layer on the dielectric layer and forming a first patterned photoresist layer on the second etching stop layer:

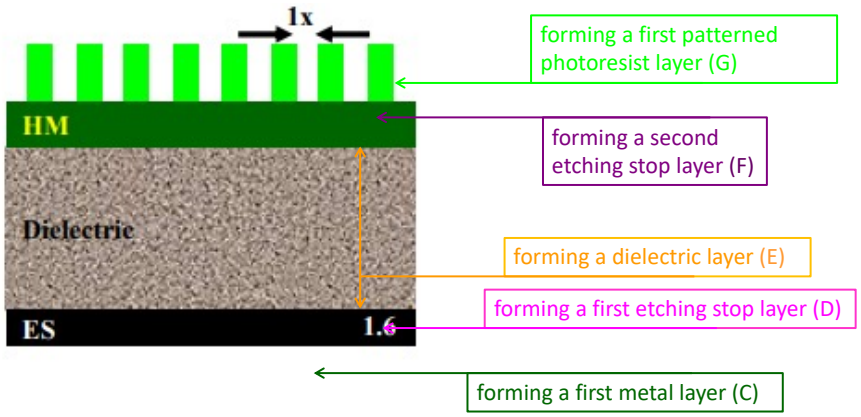

Figure 8: Schematic Drawing of the Intel’s Trench First Dual Damascene using Hardmask

65. The ’821 Exemplary Accused Product is made by forming a trench by etching through the second etching stop layer and stopping in the dielectric layer at a predetermined depth:

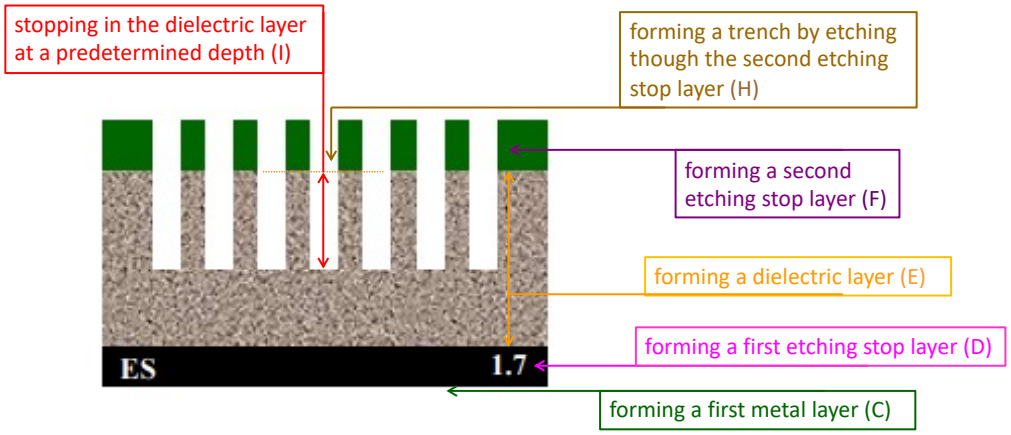

Figure 9: Schematic Drawing of the Intel’s Trench First Dual Damascene using Hardmask

66. The '821 Exemplary Accused Product is made by filling with a sacrificial layer into the trench, planarizing the sacrificial layer, and forming a second patterned photoresist layer on the sacrificial layer:

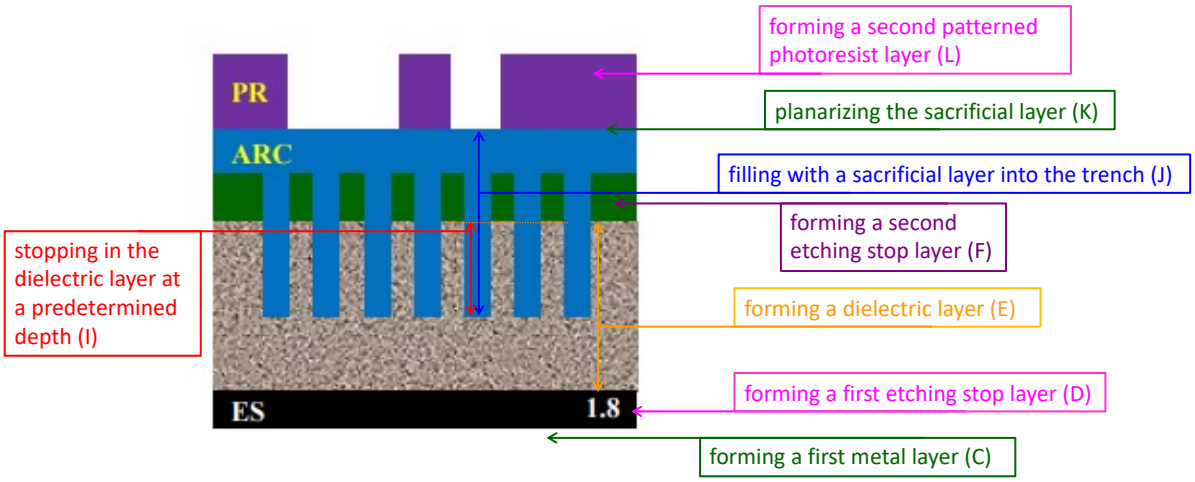

Figure 10: Schematic Drawing of the Intel's Trench First Dual Damascene using Hardmask

67. The '821 Exemplary Accused Product is made by forming a via by etching the sacrificial layer and the dielectric layer and removing the sacrificial layer and the second patterned photoresist layer:

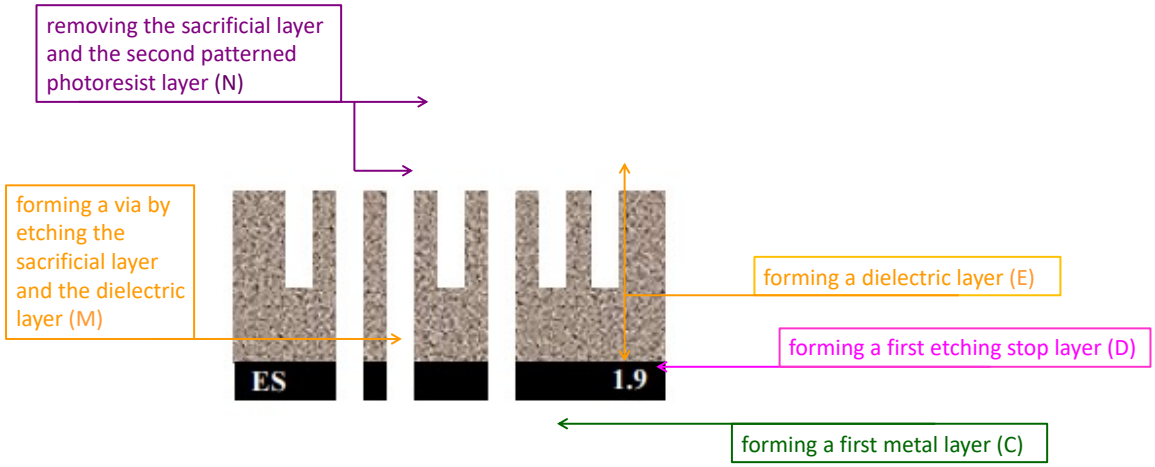

Figure 11: Schematic Drawing of the Intel's Trench First Dual Damascene using Hardmask

68. The '821 Exemplary Accused Product is made by etching the first etching stop layer to expose the first metal layer:

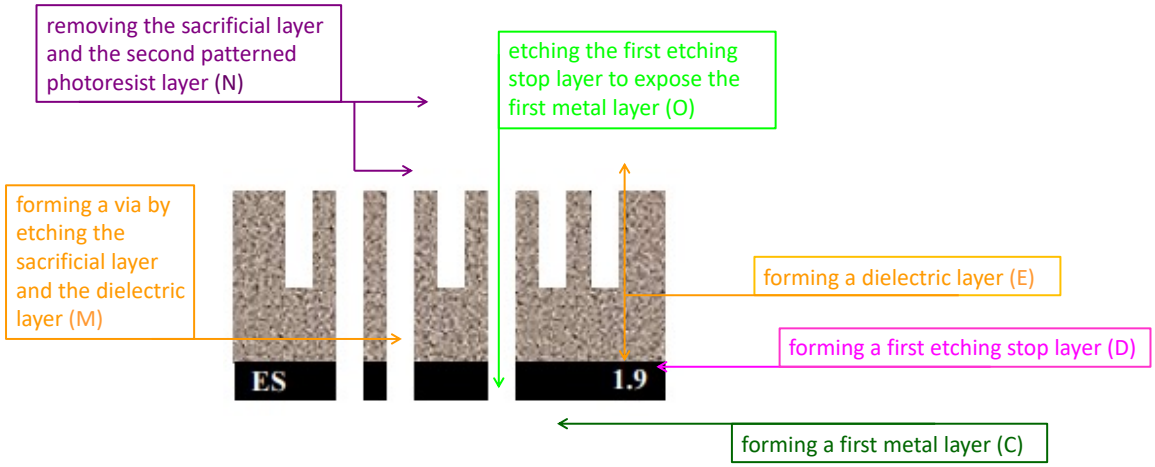

Figure 12: Schematic Drawing of the Intel's Trench First Dual Damascene using Hardmask

69. The '821 Exemplary Accused Product is made by filling with a second metal layer and planarizing the second metal layer:

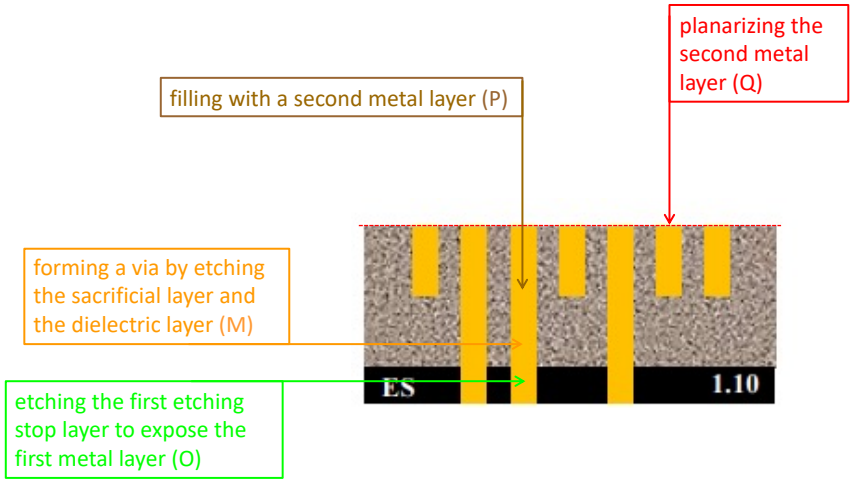

Figure 13: Schematic Drawing of the Intel's Trench First Dual Damascene using Hardmask

Willful Infringement

70. Defendant had actual knowledge of the '821 Patent and its infringement thereof at least as of receipt of Plaintiff's notice letters dated April 19, 2020 and/or March 26, 2021.

71. Defendant has numerous lawyers and other active agents of Defendant who regularly review patents and published patent applications relevant to technology in the fields of the Asserted Patents.

72. Defendant has been issued many thousands of patents held in the name of the Defendant or a related entity, many of which are patents prosecuted in the USPTO in the same technology area as the '821 Patent, giving Defendant intimate knowledge of the art in fields relevant to this civil action. The timing, circumstances and extent of Defendant obtaining actual knowledge of the '821 Patent prior to the commencement of this lawsuit will be confirmed during discovery.

73. Defendant's infringement of the Asserted Patents was either known or was so obvious that it should have been known to Defendant.

74. Notwithstanding this knowledge, Defendant has knowingly or with reckless disregard infringed the '821 Patent. Defendant continued to commit acts of infringement despite being on notice of an objectively high likelihood that its actions constitute infringement of Plaintiff's valid patent rights, either literally or equivalently.

75. Defendant is therefore liable for willful infringement and Plaintiff accordingly seeks enhanced damages pursuant to 35 U.S.C. §§ 284 and 285.

Indirect, Induced, and Contributory Infringement

76. Defendant, directly and/or through its subsidiaries, affiliates, agents, and/or business partners, has committed and continues to commit acts of indirect infringement of at least one claim of the '821 Patent, pursuant to 35 U.S.C. §§ 271(b) and (c) by actively inducing or contributing to the acts of direct infringement performed by others in the United States, the State of Texas, and the Western District of Texas.

77. Defendant has induced and continues to induce through affirmative acts its distributors, manufacturers, testers, customers, and/or end users, such as designers of Defendant's chips and end users of Defendant's chips to directly infringe the '821 Patent by making, using, selling, and/or importing the '821 Accused Products, with the specific intent to induce acts constituting infringement, and knowing that the induced acts constitute patent infringement, either literally or equivalently.

78. Defendant has knowingly contributed to direct infringement by its customers through affirmative acts and by having imported, sold, and/or offered for sale, and knowingly importing, selling, and/or offering to sell within the United States the '821 Accused Products which are not suitable for substantial non-infringing use and which are especially made or especially adapted for use by its customers in an infringement of the asserted patent.

79. The affirmative acts of inducement by Defendant include, but are not limited to, any one or a combination of: (i) designing infringing chips for manufacture

according to specification; (ii) collaborating on and/or funding the development of the infringing chips and/or technology; (iii) soliciting and sourcing the manufacture of infringing chips; licensing and transferring technology and know-how to enable the manufacture of infringing chips; (v) enabling and encouraging the use, sale, or importation of infringing chips by its customers; (vi) advertising the infringing chips and/or technology; and (vii) providing data sheets, technical guides, demonstrations, software and hardware specifications, installation guides, product specifications, user manuals, marketing materials, and instructions, including on Defendant's website, https://www.intel.com.

80. Defendant has contributed and continues to contribute to the direct infringement of the '821 Patent by its customers, and other third parties; and Defendant, its customers, and other third parties do directly infringe.

81. Defendant imports, exports, makes or sells parts, components, or intermediate products to customers and third parties that, once assembled, infringe upon the '821 Patent by the sale and/or use of the assembled processors and/or devices.

82. Defendant makes, uses, sells, and/or offers to sell infringing semiconductor devices and/or processor chips, which are especially made to design and specification, and are not staple products or commodities with substantial non-infringing use.

83. Defendant knew that the induced conduct would constitute infringement and intended that infringement at the time of committing the

aforementioned acts, such that the acts and conduct have been and continue to be committed with the specific intent to induce infringement, or deliberately avoiding learning of the infringing circumstances at the time of committing these acts so as to be willfully blind to the infringement that was induced.

84. As a result of Defendant's infringement, Plaintiff has suffered monetary damages, and is entitled to an award of damages adequate to compensate it for such infringement which, by law, can be no less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 US.C. § 284.

85. Plaintiff has incurred and will continue to incur substantial damages, including monetary damages.

COUNT THREE
INFRINGEMENT OF U.S. PATENT 7,498,642

86. Plaintiff incorporates by reference the allegations in all preceding paragraphs as if fully set forth herein.

87. The '642 Patent, entitled "PROFILE CONFINEMENT TO IMPROVE TRANSISTOR PERFORMANCE," was filed on April 25, 2005 and duly and legally issued by the United States Patent and Trademark Office on March 3, 2009.

88. The '642 Patent claims patent-eligible subject matter and is valid and enforceable.

Technical Description and Background

89. The '642 Patent is directed to a semiconductor device with well-defined profiles, specifically to profile confinement of source/drain regions and gates. According to the Patent '642, "it is difficult to confine the boron/BF_2 within the desired

locations to effectively neutralize the lateral diffusion of the n-type dopants. Having high diffusibility, boron and BF_2 dopants diffuse away easily from original implanted regions during subsequent processes that require elevated temperatures, such as rapid thermal annealing (RTA) steps. Therefore, the p-type dopant's ability to neutralize the n-type dopants diffused from source/drain regions is reduced." '642 Patent, 1:29-36.

90. However, according to the '642 Patent, "nitrogen, carbon, and fluorine have the function of retarding the diffusion of respective dopants. Therefore, the diffusion of the dopants is controlled when annealed, and thus the [lightly diffused source/drain] (LDD) regions have higher impurity concentrations and more confined profiles." '642 Patent, 1:52-56. "The addition of carbon or fluorine makes relatively high concentrations of phosphorus possible since less is diffused away, and transistor drive current is improved without unduly compromising the short channel characteristics." '642 Patent, 1:66-2:3. According to the '642 Patent, the problem is that "the same approaches are less effective in suppressing lateral diffusion of the dopants into the channel region. A method of suppressing lateral diffusion to improve the short channel characteristics of [negative metal oxide semiconductor] (NMOS) devices, therefore, is needed." '642 Patent, 2:7-11.

91. A solution to the aforementioned problem is forming a p-type pocket halo region "preferably along a channel-side border of the N+ S/D region, to neutralize diffused n-type elements from the N+ S/D region. A diffusion-retarding region is formed to retard diffusion of both p-type and n-type impurities. The diffusion-

retarding region is preferably tilt implanted to extend under the gate electrode." '642 Patent, 2:19-25. It is preferred to form the diffusion-retarding region in the gate electrode to reduce the diffusion of n-type impurities into the gate dielectric, and to preserve gate oxide integrity. '642 Patent, 2:29-32.

Direct Infringement

92. Defendant without authorization or license from Plaintiff has directly infringed the '642 Patent, either literally or equivalently, as infringement is defined by 35 U.S.C. § 271, including through making, using (including for testing purposes), designing, manufacturing, importing, distributing, selling, and offering for sale electronic devices and products that infringe one or more claims of the '642 Patent. Defendant is thus liable for direct infringement pursuant to 35 U.S.C. § 271.

93. Exemplary infringing products include Intel processors and chips, including but not limited to Intel's integrated circuit devices made using the Intel 45 nm and 32 nm process nodes as with, for example, Intel® Itanium® Processor 9740 using Intel's 32 nm node high-k metal gate (HKMG) CMOS process, and any other Intel products in which a diffusion-retarding region is formed to retard diffusion for impurities by substantially overlapping or extending beyond the pocket/halo region and the source/drain region at least on the channel side, and similar products, hereinafter "'642 Accused Products."

94. Plaintiff names these exemplary infringing instrumentalities to serve as notice of Defendant's infringing acts, but Plaintiff reserves the right to name

additional infringing products, known to or learned by Plaintiff or revealed during discovery, and include them in the definition of '642 Accused Products.

95. As a specific, nonlimiting example, Defendant is liable for direct infringement pursuant to 35 U.S.C. § 271 for the manufacture, sale, offer for sale, importation, or distribution of the Intel 32 nm Logic Process Technology, hereinafter "'642 Exemplary Accused Product." The '642 Exemplary Accused Product is made by a method that meets all limitations of, for example, claim 11 of the '642 Patent, either literally or under the doctrine of equivalents.

96. The '642 Exemplary Accused Product is a device comprising a substrate; a diffusion-retarding region in the substrate, wherein the diffusion-retarding region comprises fluorine:

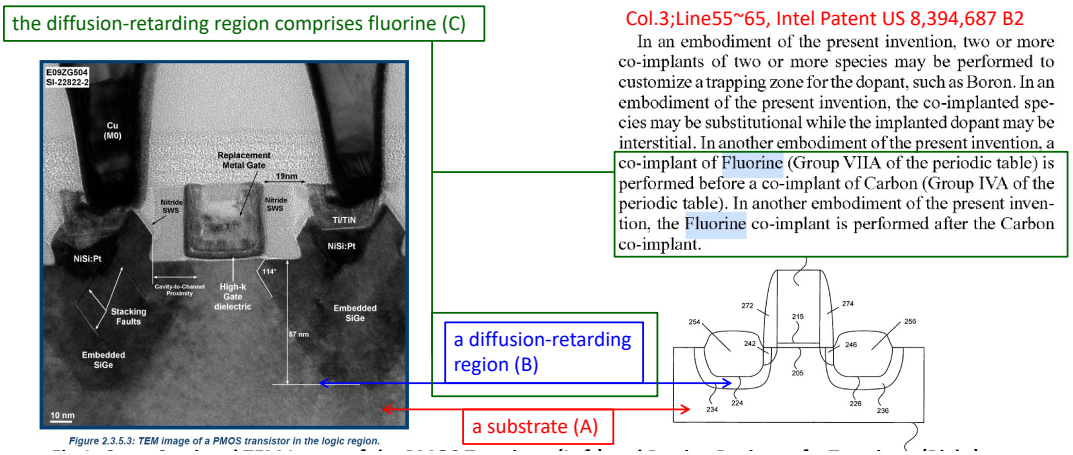

Figure 14: Cross-Sectional TEM Image of the PMOS Transistor (Left) and Doping Regions of a Transistor (Right)

97. The '642 Exemplary Accused Product is a device comprising a source/drain region of a first conductivity type in the substrate and substantially contained within the diffusion-retarding region:

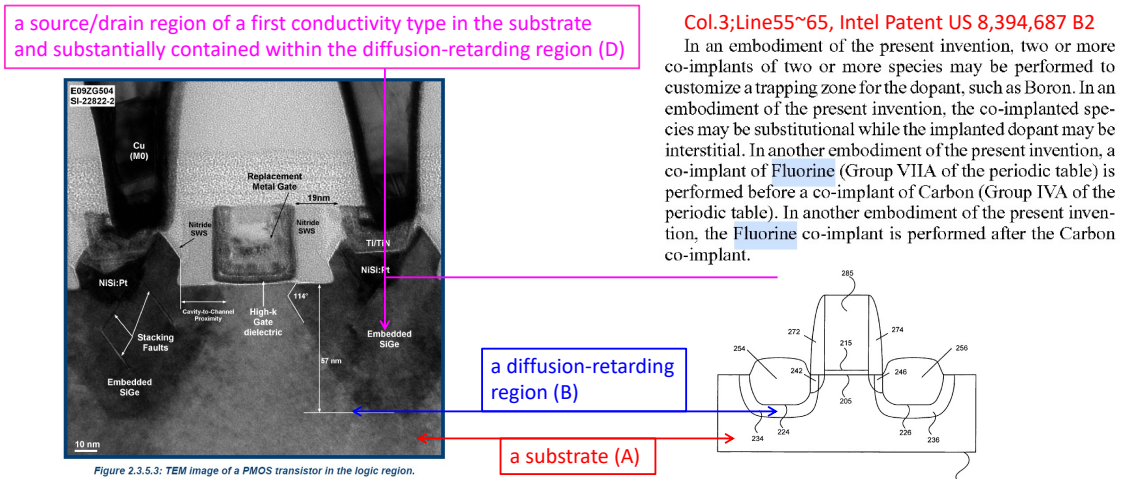

Figure 15: Cross-Sectional TEM Image of the PMOS Transistor (Left) and Doping Regions of a Transistor (Right)

98. The '642 Exemplary Accused Product is a device comprising a pocket/halo region of an opposite conductivity type formed substantially adjacent an interface of the source/drain region and the substrate, the pocket/halo region being substantially contained within the diffusion-retarding region:

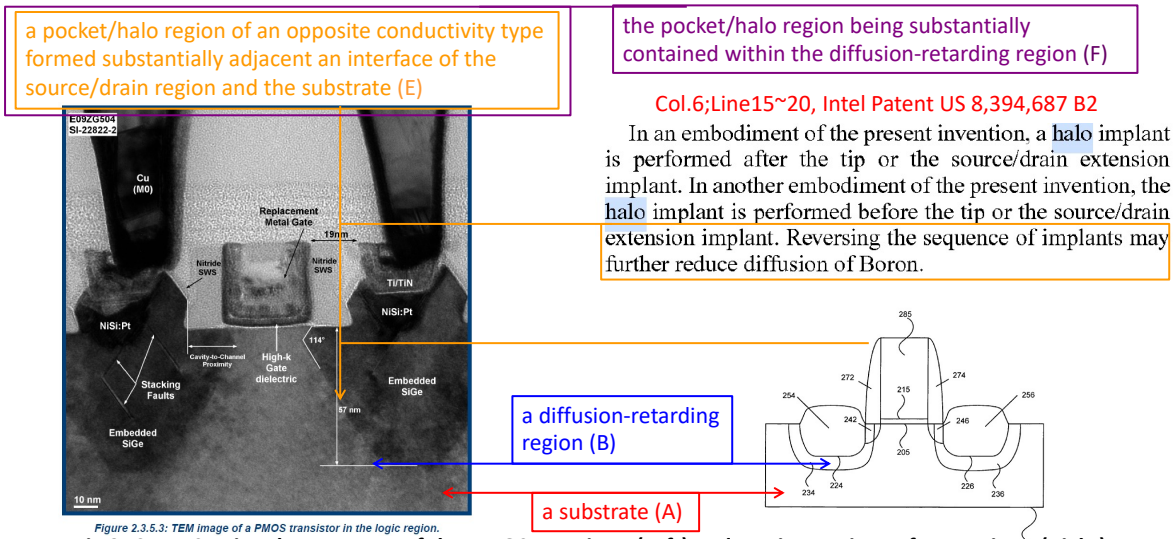

Figure 16: Cross-Sectional TEM Image of the PMOS Transistor (Left) and Doping Regions of a Transistor (Right)

Willful Infringement

99. Defendant had actual knowledge of the '642 Patent and its infringement thereof at least as of receipt of Plaintiff's notice letters dated April 19, 2020 and/or March 26, 2021.

100. Defendant has numerous lawyers and other active agents of Defendant who regularly review patents and published patent applications relevant to technology in the fields of the Asserted Patents.

101. Defendant has been issued many thousands of patents held in the name of the Defendant or a related entity, many of which are patents prosecuted in the USPTO in the same technology area as the '642 Patent, giving Defendant intimate knowledge of the art in fields relevant to this civil action. The timing, circumstances and extent of Defendant obtaining actual knowledge of the '642 Patent prior to the commencement of this lawsuit will be confirmed during discovery.

102. Defendant's infringement of the Asserted Patents was either known or was so obvious that it should have been known to Defendant.

103. Notwithstanding this knowledge, Defendant has knowingly or with reckless disregard infringed the '642 Patent. Defendant continued to commit acts of infringement despite being on notice of an objectively high likelihood that its actions constitute infringement of Plaintiff's valid patent rights, either literally or equivalently.

104. Defendant is therefore liable for willful infringement and Plaintiff accordingly seeks enhanced damages pursuant to 35 U.S.C. §§ 284 and 285.

Indirect, Induced, and Contributory Infringement

105. Defendant, directly and/or through its subsidiaries, affiliates, agents, and/or business partners, has committed and continues to commit acts of indirect infringement of at least one claim of the '642 Patent, pursuant to 35 U.S.C. §§ 271(b) and (c) by actively inducing or contributing to the acts of direct infringement performed by others in the United States, the State of Texas, and the Western District of Texas.

106. Defendant has induced and continues to induce through affirmative acts its distributors, manufacturers, testers, customers, and/or end users, such as designers of Defendant's chips and end users of Defendant's chips to directly infringe the '642 Patent by making, using, selling, and/or importing the '642 Accused Products, with the specific intent to induce acts constituting infringement, and knowing that the induced acts constitute patent infringement, either literally or equivalently.

107. Defendant has knowingly contributed to direct infringement by its customers through affirmative acts and by having imported, sold, and/or offered for sale, and knowingly importing, selling, and/or offering to sell within the United States the '642 Accused Products which are not suitable for substantial non-infringing use and which are especially made or especially adapted for use by its customers in an infringement of the asserted patent.

108. The affirmative acts of inducement by Defendant include, but are not limited to, any one or a combination of: (i) designing infringing chips for manufacture

according to specification; (ii) collaborating on and/or funding the development of the infringing chips and/or technology; (iii) soliciting and sourcing the manufacture of infringing chips; licensing and transferring technology and know-how to enable the manufacture of infringing chips; (v) enabling and encouraging the use, sale, or importation of infringing chips; enabling and encouraging the use, sale, or importation of infringing chip by its customers; (vi) advertising the infringing chips and/or technology; and (vii) providing data sheets, technical guides, demonstrations, software and hardware specifications, installation guides, product specifications, user manuals, marketing materials, and instructions, including on Defendant's website, https://www.intel.com.

109. Defendant has contributed and continues to contribute to the direct infringement of the '642 Patent by its customers, and other third parties, and Defendant, its customers, and other third parties do directly infringe.

110. Defendant imports, exports, makes or sells parts, components, or intermediate products to customers and third parties that, once assembled, infringe upon the '642 Patent by the sale and/or use of the assembled processors and/or devices.

111. Defendant makes, uses, sells, and/or offers to sell infringing semiconductor devices and/or processor chips, which are especially made to design and specification, and are not staple products or commodities with substantial non-infringing use.

112. Defendant knew that the induced conduct would constitute infringement and intended that infringement at the time of committing the aforementioned acts, such that the acts and conduct have been and continue to be committed with the specific intent to induce infringement, or deliberately avoiding learning of the infringing circumstances at the time of committing these acts so as to be willfully blind to the infringement that was induced.

113. As a result of Defendant's infringement, Plaintiff has suffered monetary damages, and is entitled to an award of damages adequate to compensate it for such infringement which, by law, can be no less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 US.C. § 284.

114. Plaintiff has incurred and will continue to incur substantial damages, including monetary damages.

COUNT FOUR
INFRINGEMENT OF U.S. PATENT 7,511,332

115. Plaintiff incorporates by reference the allegations in all preceding paragraphs as if fully set forth herein.

116. The '332 Patent, entitled "VERTICAL FLASH MEMORY," was filed on August 29, 2005 and duly and legally issued by the United States Patent and Trademark Office on March 31, 2009.

117. The '332 Patent claims patent-eligible subject matter and is valid and enforceable.

Technical Description and Background

118. The ’332 Patent is directed to flash memory cells with vertical transistors. Transistors are semiconductor devices that are formed on wafers, which are made by foundries. Wafers contain multiple, identical chips which are designed by chip designers. Individual chips are cut from wafers and packaged. Those chips go into a variety of consumer products, such as smartphones, tablets, personal computers, and automobile parts and components.

119. According to the ’332 Patent, in a flash memory cell, “a thin layer of oxide is deposited as tunnel oxide on top of a channel area on a p-type silicon substrate (P—Si). A layer of poly-silicon is deposited on top of the tunnel oxide as a floating gate (FG). Another layer of oxide is deposited on top of the floating gate (FG) as an isolation layer. A front metal-based gate is deposited on top of the isolation oxide for voltage control, i.e. a control gate (CG). The silicon substrate (P—Si) beside the gate structure is doped with n-type ions to serve as source/drain regions (S/D). Because the floating gate is insulated by oxide, negative charge thereon is contained, even if power is interrupted.” ’332 Patent, 1:26-36.

120. As explained in the ’332 Patent, conventional flash memory cells were limited by a minimum lithographic feature size, but there was an ongoing increasing demand for high-capacity memory devices. Thus, there was a need to develop denser flash memory devices. ’332 Patent, 1:48-51.

121. The ’332 Patent improved upon the prior art by disclosing a new technology to provide a vertical flash memory cell structure and a stackable flash

memory array to increase the storage capacity of the flash memory. '332 Patent, 1:55-58. "Based on the array of vertical flash memory cells, the present invention further provides a multi-level structure of flash memory arrays. A first level of the array of vertical flash memory cells as previously described are disposed on a substrate. A second level of the same array of vertical flash memory cells is then disposed on the first level. Thus, a stackable flash memory device with increased storage capacity is achieved." '332 Patent, 2:35-44.

Direct Infringement

122. Defendant without authorization or license from Plaintiff, has been and is directly infringing the '332 Patent, either literally or equivalently, as infringement is defined by 35 U.S.C. § 271, including through making, using (including for testing purposes), designing, manufacturing, importing, distributing, selling, and offering for sale chips, memory, and other electronic devices and products that infringe one or more claims of the '332 Patent. Defendant is thus liable for direct infringement pursuant to 35 U.S.C. § 271.

123. Exemplary infringing products include at least all Intel integrated circuit devices made using the vertical array of flash memory cells, as shown, for example, in the Intel B17A 512Gb using Intel's 20 nm 64L 3D2 NAND triple-level cell (TLC) CMOS process in which the vertical NAND flash memory cells are manufactured to provide a stackable flash memory array to increase storage capacity, and similar products, hereinafter "'332 Accused Products."

124. Plaintiff names these exemplary infringing instrumentalities to serve as notice of Defendant's infringing acts, but Plaintiff reserves the right to name additional infringing products, known to or learned by Plaintiff or revealed during discovery, and include them in the definition of '332 Accused Products.

125. As a specific, nonlimiting example, Defendant is liable for direct infringement pursuant to 35 U.S.C. § 271 for the manufacture, sale, offer for sale, importation, or distribution of the Intel 29F01T2ANCTH264-Layer 256 Gb 3D NAND Flash, hereinafter "'332 Exemplary Accused Product." The '332 Exemplary Accused Product meets all limitations of, for example, claim 1 of the '332 Patent, either literally or under the doctrine of equivalents.

126. The '332 Exemplary Accused Product is flash memory device, comprising a memory cell, which comprises a substrate with a first insulating layer disposed thereon:

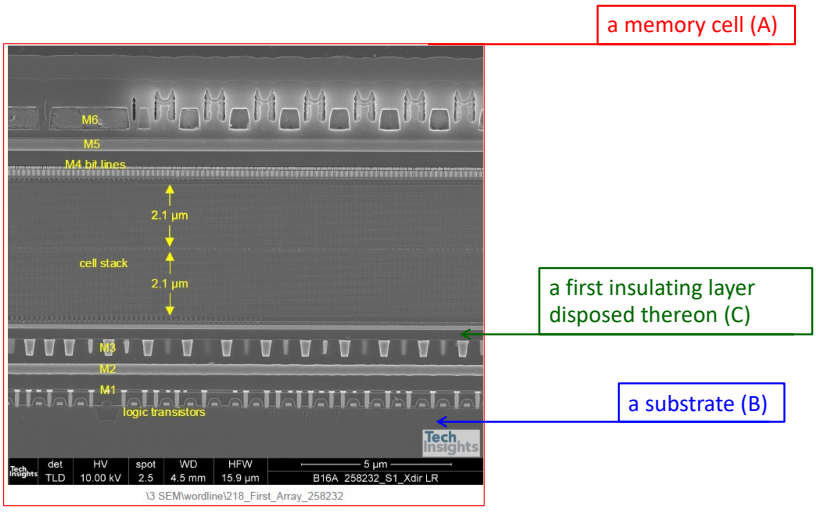

Figure 17: Cross-Sectional SEM the Intel 64L 3D NAND Memory Cell

127. The ’332 Exemplary Accused Product is flash memory device, comprising a memory cell, which comprises a source region, channel region and drain region stacked on the substrate sequentially as a transistor body; a tunnel dielectric layer on a sidewall of the transistor body; a floating gate disposed on the tunnel dielectric layer:

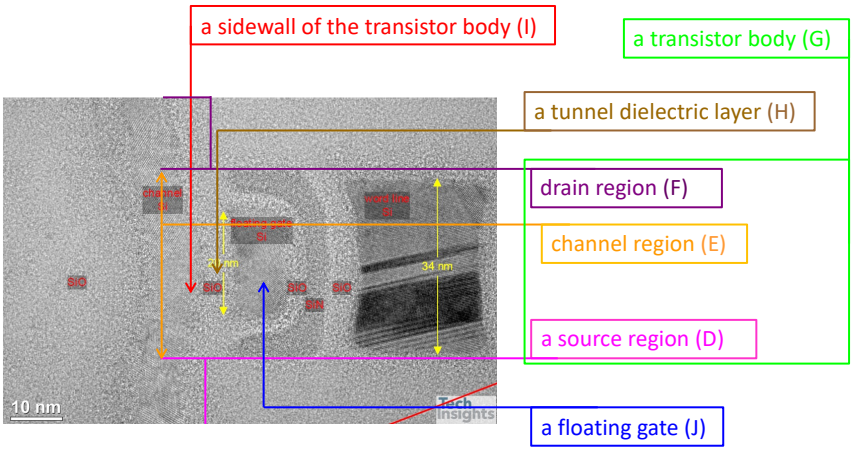

Figure 18: High magnification view of the Intel 64L 3D NAND cell (TEM)

128. The ’332 Exemplary Accused Product is flash memory device, comprising a memory cell, which comprises a second insulating layer covering the floating gate; a control gate disposed on the second insulating layer, isolated from the floating gate by the second insulating layer and from the transistor body by the tunnel dielectric layer:

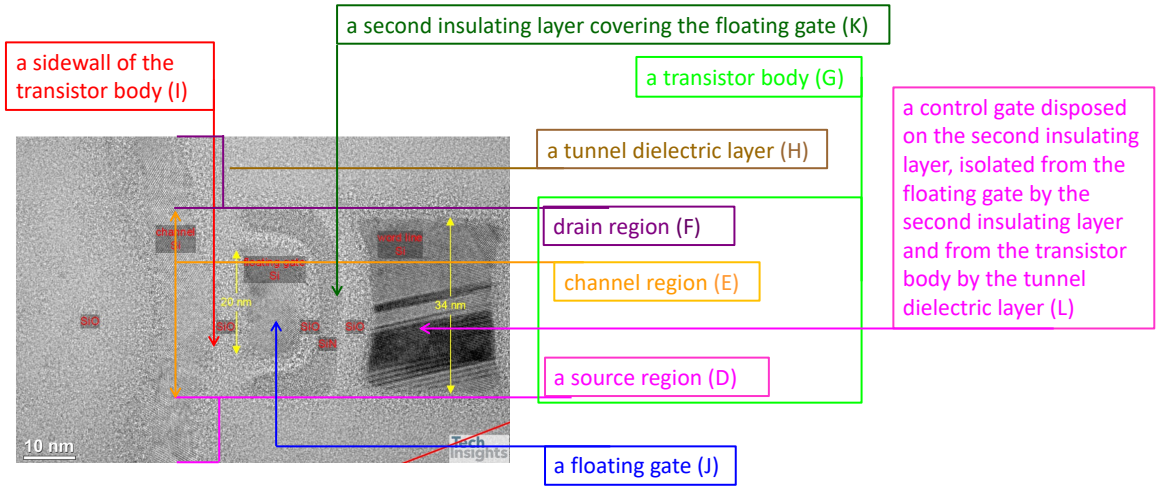

Figure 19: High magnification view of the Intel 64L 3D NAND cell (TEM)

129. The '332 Exemplary Accused Product is flash memory device, comprising a memory cell, which comprises a bit line electrically connected to the top of the transistor body via a bit line contact plug:

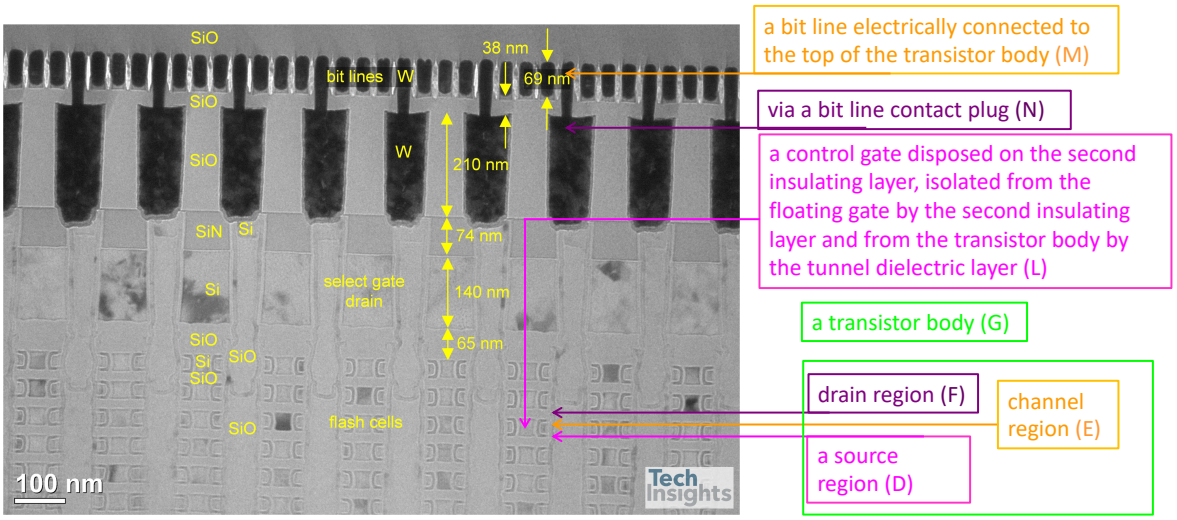

Figure 20: Intel 64L 3D NAND cells at top of vertical NAND string (TEM)

130. The '332 Exemplary Accused Product is flash memory device, comprising a memory cell, which comprises a word line electrically connected to the

control gate via a word line contact plug, wherein the bit line and word line are isolated by a third insulating layer:

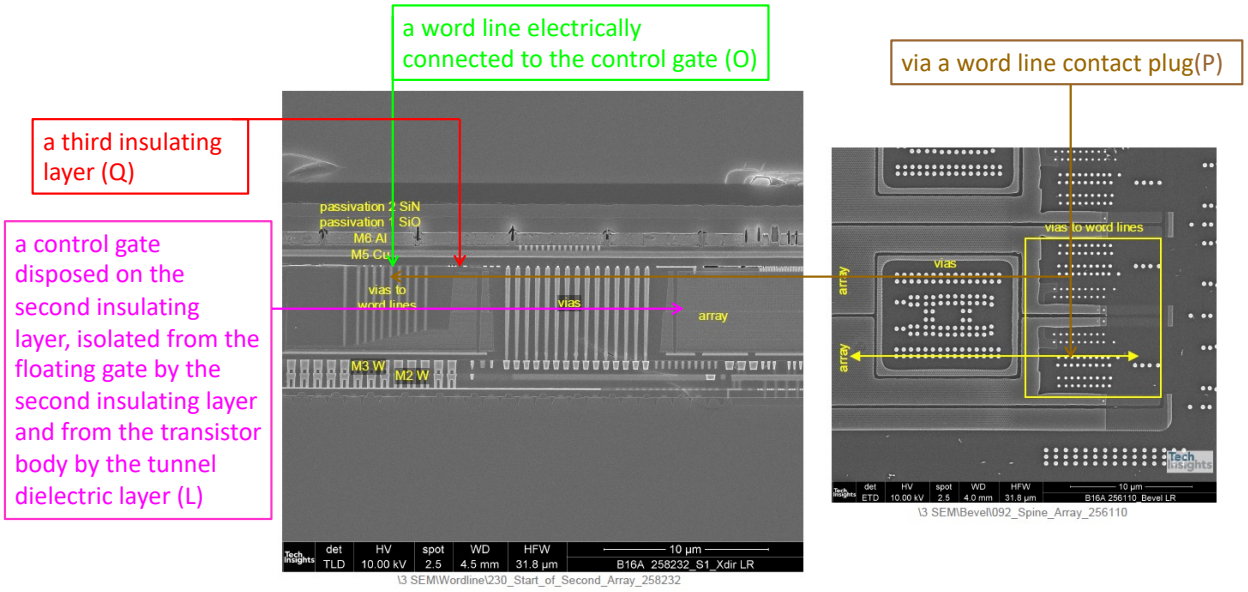

Figure 21: Word Line Contacts: Cross-Sectional SEM Image (Left), and Plan View SEM Image (Right)

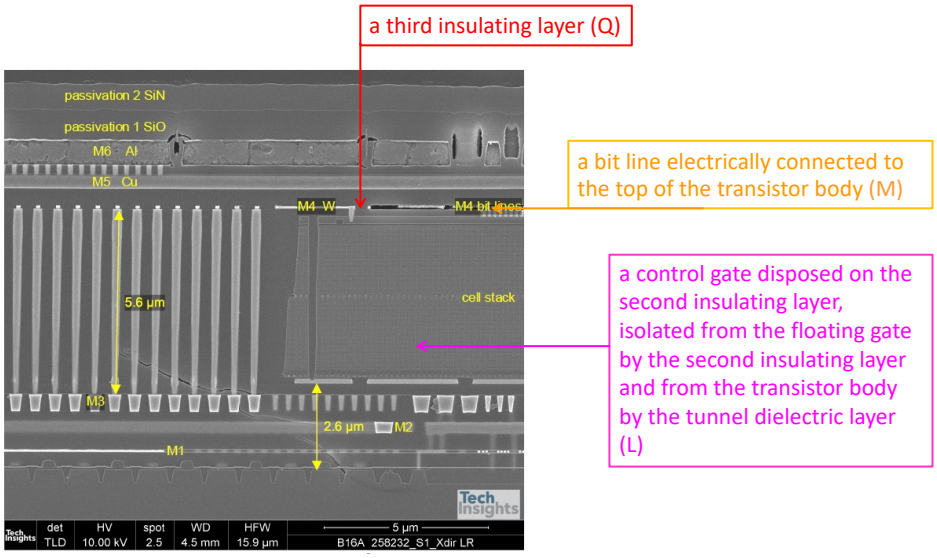

Figure 21-1: Cross-Sectional SEM Image of the Intel 64L 3D NAND Cell

131. The '332 Exemplary Accused Product is flash memory device, comprising a memory cell, which comprises a source line disposed in the first insulating layer of the substrate, in contact with the source region:

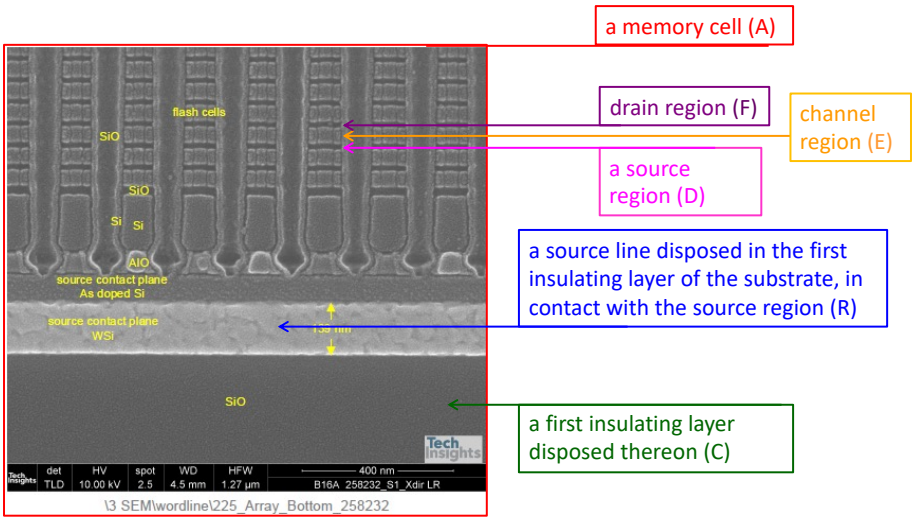

Figure 22: Intel 64L 3D NAND cells at Bottom of vertical NAND string (SEM)

132. The top of the floating gate is between the upper and bottom surface of the channel regions and the top of the control gate is not over the upper surface of the channel region:

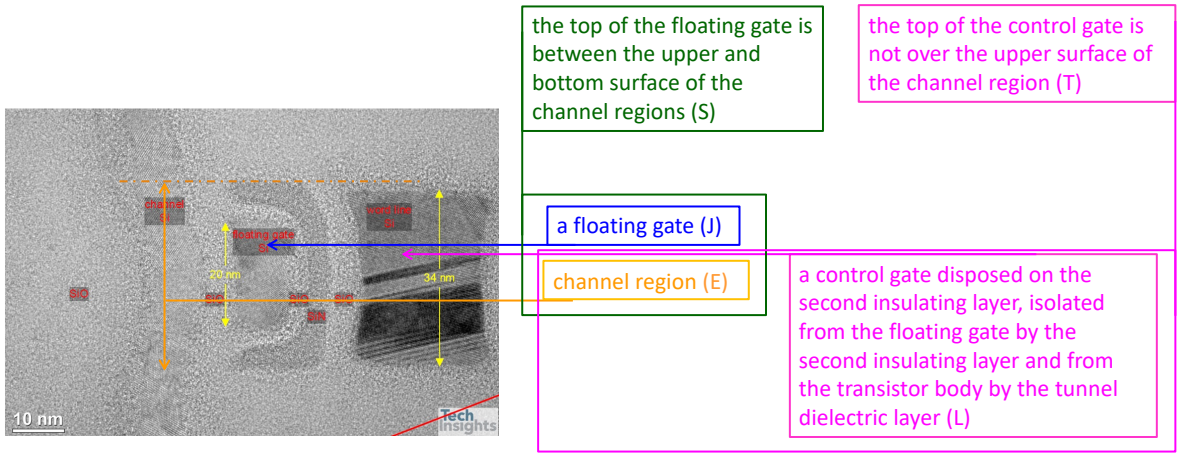

Figure 23: High magnification view of an Intel 64L 3D NAND cell (TEM)

Willful Infringement

133. Defendant had actual knowledge of the '332 Patent and its infringement thereof at least as of receipt of Plaintiff's notice letters dated April 19, 2020 and/or March 26, 2021.

134. Defendant has numerous lawyers and other active agents of Defendant who regularly review patents and published patent applications relevant to technology in the fields of the Asserted Patent.

135. Defendant has been issued many thousands of patents held in the name of the Defendant or a related entity, many of which are patents prosecuted in the USPTO in the same technology area as the '332 Patent, giving Defendant intimate knowledge of the art in fields relevant to this civil action. The timing, circumstances and extent of Defendant obtaining actual knowledge of the '332 Patent prior to the commencement of this lawsuit will be confirmed during discovery.

136. Defendant's infringement of the Asserted Patents was either known or was so obvious that it should have been known to Defendant.

137. Notwithstanding this knowledge, Defendant has knowingly or with reckless disregard infringed the '332 Patent. Defendant continued to commit acts of infringement despite being on notice of infringement and aware of an objectively high likelihood that its actions constitute infringement of Plaintiff's valid patent rights, either literally or equivalently.

138. Defendant is therefore liable for willful infringement and Plaintiff accordingly seeks enhanced damages pursuant to 35 U.S.C. §§ 284 and 285.

Indirect, Induced, and Contributory Infringement

139. Defendant, directly and/or through its subsidiaries, affiliates, agents, and/or business partners, has committed and continues to commit acts of indirect infringement of at least one claim of the '332 Patent, pursuant to 35 U.S.C. §§ 271(b) and (c) by actively inducing or contributing to the acts of direct infringement performed by others in the United States, the State of Texas, and the Western District of Texas.

140. Defendant has induced and continue to induce through affirmative acts its distributors, manufacturers, testers, customers, and/or end users, such as designers of Defendant's chips and end users of Defendant's chips to directly infringe the '332 Patent by making, using, selling, and/or importing the '332 Accused Products, with the specific intent to induce acts constituting infringement, and knowing that the induced acts constitute patent infringement, either literally or equivalently.

141. Defendant has knowingly contributed to direct infringement by its customers through affirmative acts and by having imported, sold, and/or offered for sale, and knowingly importing, selling, and/or offering to sell within the United States the '332 Accused Products which are not suitable for substantial non-infringing use and which are especially made or especially adapted for use by its customers in an infringement of the asserted patent.

142. The affirmative acts of inducement by Defendant include, but are not limited to, any one or a combination of: (i) designing infringing chips for manufacture

according to specification; (ii) collaborating on and/or funding the development of the infringing chips and/or technology; (iii) soliciting and sourcing the manufacture of infringing chips; licensing and transferring technology and know-how to enable the manufacture of infringing chips; (v) enabling and encouraging the use, sale, or importation of infringing chips by its customers; (vi) advertising the infringing chips and/or technology; and (vii) providing data sheets, technical guides, demonstrations, software and hardware specifications, installation guides, product specifications, user manuals, marketing materials, and instructions, including on Defendant's website, https://www.intel.com.

143. Defendant has contributed and continue to contribute to the direct infringement of the '332 Patent its customers, and other third parties; and Defendant, its customers, and other third parties do directly infringe.

144. Defendant imports, exports, makes or sells parts, components, or intermediate products to customers and third parties that, once assembled, infringe the '332 Patent by the sale and/or use of the assembled chips and/or devices.

145. Defendant makes, uses, sells, and/or offers to sell infringing semiconductor devices and/or chips, which are especially made to design and specification, and are not staple products or commodities with substantial non-infringing use.

146. Defendant knew that the induced conduct would constitute infringement and intended that infringement at the time of committing the aforementioned acts, such that the acts and conduct have been and continue to be

committed with the specific intent to induce infringement, or deliberately avoiding learning of the infringing circumstances at the time of committing these acts so as to be willfully blind to the infringement that was induced.

147. As a result of Defendant's infringement, Plaintiff has suffered monetary damages, and is entitled to an award of damages adequate to compensate it for such infringement which, by law, can be no less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 US.C. § 284.

148. Plaintiff has incurred and will continue to incur substantial damages, including monetary damages.

149. Plaintiff has been and continues to be irreparably harmed by Defendant's infringement of the '332 Patent.

150. Therefore, Plaintiff is entitled to an injunction, actual and/or compensatory damages, reasonable royalties, pre-judgment and post-judgment interest, enhanced damages, and costs.

V. NOTICE

151. Trenchant has complied with the notice requirement of 35 U.S.C. § 287 and does not currently distribute, sell, offer for sale, or make products embodying the Asserted Patents. This notice requirement has been complied with by all relevant persons at all relevant times.

152. Defendant had actual knowledge of the Asserted Patents and its infringement thereof at least as of receipt of Plaintiff's notice letters dated April 19, 2020 and/or March 26, 2021.

VI. JURY DEMAND

153. Plaintiff Trenchant demands a trial by jury of all matters to which it is entitled to trial by jury, pursuant to Fed. R. Civ. P. 38.

VII. PRAYER FOR RELIEF

WHEREFORE, Plaintiff Trenchant prays for judgment and seeks relief against Defendant as follows:

A. A judgment in favor of Plaintiff that Defendant has directly infringed, and/or has indirectly infringed by way of inducement and/or contributory infringement, one or more claims of the Asserted Patents;

B. A judgment that Defendant's infringement has been willful;

C. A judgment that Plaintiff has been irreparably harmed by Defendant's infringing activities and is likely to continue to be irreparably harmed by Defendant's continued infringement;

D. Preliminary and permanent injunctions prohibiting Defendant and its officers, agents, servants, employees, and those persons in active concert or participation with Defendant, as well as all successors or assignees of the interests or assets related to the Accused Instrumentalities, from further infringement, direct or indirect, of the Asserted Patents;

E. A judgment and order requiring Defendant to pay Plaintiff damages adequate to compensate for infringement under 35 U.S.C. § 284, which damages in no event shall be less than a reasonable royalty for the use made

of the inventions of the Asserted Patents, including pre- and post-judgment interest and costs, including expenses and disbursements;

F. A judgment and order requiring Defendant to pay Plaintiff enhanced damages pursuant to 35 U.S.C. § 284;

G. A judgment and order finding this case exceptional pursuant to 35 U.S.C. § 285; and

H. Any and all such further necessary relief as the Court may deem just and proper under the circumstances.

VIII. RESERVATION OF RIGHTS

Plaintiff's investigation is ongoing, and certain material information remains in the sole possession of Defendant or third parties, which will be obtained via discovery herein. Plaintiff expressly reserves the right to amend or supplement the causes of action set forth herein in accordance with FED. R. CIV. P. 15.

Dated: May 11, 2021

Respectfully Submitted,

/s/ Scott W. Breedlove

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